

CROSSTALK MINIMIZATION IN SERIAL LINK SYSTEMS

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FIELD OF THE INVENTION

[0001] The present invention relates generally to the field of communications, and more particularly to noise abatement for high speed electronic signaling within and between integrated circuit devices.

BACKGROUND

[0002] Figure 1 (prior art) depicts a conventional backplane communication system 100. Communication system 100 includes a pair of line cards 105 connected to a backplane 115 via a respective pair of backplane connectors 120. Each of line cards 105 supports a corresponding integrated circuit 125 mounted within a package 135. Integrated circuits 125 communicate via communication channels, or “links,” made up of line-card traces 145, connectors 120, and backplane traces 150 as well as other sub-components such as inter-layer vias, etc.

[0003] Integrated circuits 125 communicate internally at very high speeds, tens of gigabits per second in some examples. The communication channels extending between integrated circuits 125 are comparatively slow, and consequently limit system speed performance. A considerable effort has been made to address this performance limitation.

[0004] System 100 of Figure 1 is simplified for ease of illustration; in a practical system, backplane 115 and line cards 105 include a complex matrix of densely populated communication channels. As a result, data transmitted on some of the communication channels electromagnetically couples into adjacent or nearby communication channels, resulting in a type of noise conventionally termed “crosstalk.” The combined crosstalk from numerous “aggressor”

channels induces data errors on one or more neighboring “victim” channels. Addressing this problem is critical to improving system speed performance while maintaining acceptable bit-error-rates “BER”. As used herein, the term aggressor channel is intended to describe the channel carrying a signal that causes a crosstalk effect in another channel, and the term victim channel is intended to describe a channel carrying a signal that experiences the effect of such crosstalk. A channel may at one time be both an aggressor channel relative to one channel and a victim channel relative to another channel. A channel may at some times be an aggressor channel and at other times a victim channel.

BRIEF DESCRIPTION OF THE FIGURES

[0005] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

[0006] Figure 1 (prior art) depicts a conventional backplane communication system 100.

[0007] Figure 2A depicts a mesochronous serial communication system 200 in accordance with one embodiment.

[0008] Figure 2B is a simple waveform diagram 270 depicting eye patterns 255, 260, and 261 associated with respective transmit data TXD1, TXDN, and TXDM of respective channels 212, 215, and 216 of Figure 2A.

[0009] Figure 2C is a waveform diagram 250 depicting the effect, from the victim receiver’s perspective, of misaligning aggressor data.

[0010] Figure 3A depicts a plesiochronous system 300 in accordance with another embodiment.

[0011] Figure 3B is a waveform diagram 350 depicting the effect of sweeping a transmit data eye 355 for the transmit data TXD1 associated with aggressor channel 212.

[0012] Figure 4 depicts a transceiver 400 in accordance with an embodiment that can be used for mesochronous and plesiochronous systems.

[0013] Figure 5 (prior art) depicts a phase mixer 500 used in some embodiments of transceiver 400 as transmit phase mixer 430.

[0014] Figure 6 depicts a communication system 600 in accordance with an embodiment in which a system phase controller 605 issues control signals Ctrl to a transmitter 610 based upon feedback signals received from one or more near-end receivers 615 and far-end receivers 620.

[0015] Figure 7 depicts a communication system 700 in accordance with an embodiment in which a system phase controller 705 issues control signals Ctrl to one or more potential aggressor transmitters 710 in response to feedback signals received from one or more far-end receivers 715.

[0016] Figure 8 depicts a multi-channel transmitter 800 that includes two (or more) collections of N transmitters 805 and 810.

DETAILED DESCRIPTION

[0017] Various embodiments of the present invention may be employed to reduce the impact of crosstalk. Communication circuits in accordance with some embodiments adjust the timing of transitions of transmitted “aggressor” data to reduce, from the perspective of potential victim receivers, the effects of crosstalk. This adjustment of the transition timing moves the noise artifacts on the coupled victim channel away from sensitive regions in the victim data, and consequently reduces the effects of crosstalk on the victim data.

[0018] Some embodiments reduce the effects of crosstalk by introducing static timing offsets to one or a plurality of aggressor transmitters, one or a plurality of victim transmitters, or some combination of aggressor and victim transmitters. Other embodiments dynamically alter the relative timing of aggressor and victim transmitters.

[0019] Some high-performance communication systems employ receivers that capture data and the associated timing from the incoming data stream. Because such receivers recover the timing from the incoming signal, the receivers do not need a reference clock signal having a phase that is fixed in relation to the phase of the incoming signal. Communication systems in accordance with some embodiments can take advantage of this phase insensitivity by adjusting the phase of transmitted aggressor data to minimize the impact of crosstalk on data on potential victim channels. Adjusting the phase, as used herein, means adjusting the timing of the clock signal that times the transmission of data, and consequently adjusting the timing of the transmitted data transitions relative to potential victim data.

[0020] Figure 2A depicts a mesochronous serial communication system 200 in accordance with one embodiment. System 200 includes an exemplary transceiver 205 (e.g. an integrated circuit on a line card) coupled to a second transceiver 210 via respective first, second, and third communication channels 212, 215, and 216. In some embodiments the links made up of channels 212, 215, and 216 and their respective transmitters and receivers are not contained in the two devices 205 & 210, but are in as few as one device or distributed across many different devices in a system. The system shown in Figure 2 is meant to be exemplary and not exclusive. Transceiver 205 includes a first transmitter 218 that receives transmit data TX1 on a corresponding first data input terminal. Transmitter 218 synchronizes the transmit data TX1 to a first transmit clock TxClk1 and conveys the resulting re-timed serial data TXD1 to a receiver 230 in transceiver 210 via channel 212. A phase-adjust circuit 220 derives transmit clock

TxC1k1 from a local reference clock LRC1, which is in turn derived from a system clock SysClk by a conventional clock synthesizer 247. Transceiver 210 also includes a clock synthesizer 248, which derives a second local reference clock LRC2 from the same system clock SysClk as synthesizer 247. A phase tracking circuit 249 associated with receiver 230 derives a channel-specific receive clock RC1 from the incoming transmit data TXD1 on channel 212. The phase adjust and phase tracking circuits of Figure 2A are simplified here for ease of illustration, but are described in more detail below in connection with Figure 4.

[0021] Transceiver 205 includes N-1 additional transmitters, though only the Nth transmitter 223 is shown. Transmitter 223, with an associated phase-adjust circuit 225, drives a respective second transmit signal TXDN to a corresponding receiver 233 of transceiver 210 via channel 215. The last communication channel 216 transmits data TXDM in the reverse direction, from a transmitter 235 with associated phase-adjust circuit 240 to a receiver 226 and associated phase tracking circuit 249. In an alternative embodiment, communication system 200 may comprise only one of the two links made up of the 223/215/233 link and the 235/216/226 link. In other alternative embodiments, communication system 200 may comprise one or more links in each direction.

[0022] Transmitter 218 and receiver 230 perceive different phases of system clock SysClk due to different propagation delays between the system clock source and the separate transceivers. This phase error does not pose a problem, however, as the receivers do not use the system clock to capture data, but instead use the system clock as a frequency reference and use standard clock and data recovery “CDR” techniques to generate local receive clock LRC1. An example of conventional receive circuitry that extracts timing and data from serial data is described below in connection with Figure 4.

[0023] The phase-adjust circuits associated with each transmitter alter the phase of the transmit clocks, and consequently the transmitted data, to reduce the impact of crosstalk. For illustrative purposes, channel 212 is assumed to be an aggressor channel that induces undesirable crosstalk into victim channels 215 and 216. Additional aggressor channels might also be included, and their separate or combined effects can exacerbate crosstalk problems. Additional aggressor channels are omitted here for ease of illustration.

[0024] System 200 addresses two distinct forms of crosstalk. The first, commonly referred to as “far-end crosstalk” (FEXT), is characterized by the crosstalk source being received at the same destination as the victim, and is illustrated by arrow 236. Signals switching on channel 212 cross-couple to channel 215 and are consequently perceived, at least in part, by receiver 233. The second form of crosstalk, commonly referred to as “near-end crosstalk” (NEXT), is characterized by the crosstalk source originating at the same location as the victim receiver, and is illustrated by an arrow 241. In that case, signals switching on channel 212 may cross-couple to channel 216 and may consequently be perceived, at least in part, by receiver 226.

[0025] Figure 2C is a simple waveform diagram 250 depicting an aggressor data symbol 255 associated with transmit data TXD1 of channel 212 and two eye diagrams 260 and 261 associated with respective transmit data TXDN and TXDM of respective channels 215 and 216. The transition times of the aggressor data, illustrated by the falling and rising edges of symbol 255, induce FEXT and NEXT artifacts 262 and 264 in nearby channels 215 and 216. If artifacts 262 and 264 are of sufficient amplitude and duration, victim receivers 226 and 233 will experience increased bit-error-rates. Artifacts 262 and 264 are particularly troublesome if they occur at the sample instants of the received victim data, typically at or near the center of eyes 260 and 261.

[0026] Returning to Figure 2A, phase-adjust circuits 220 and 225 can alter the transmit timing of the aggressor data symbol 255 and victim data eye 260. Offsetting the timing of data transmitted on one or more aggressor channels with respect to data transmitted on one or more victim channels can reduce the impact of the aggressor data on the victim data. Figure 2B is a waveform diagram 270 depicting this desirable effect. In this example, the timing of data symbol 255 is altered, as compared with the example of Figure 2C, with respect to victim eye diagrams 260 and 261. Artifacts 262 and 264 are thus offset with respect to the sampling instants of the received victim data 260 and 264 to instants at which the victim channels are less sensitive to crosstalk. The detrimental impact of NEXT and FEXT is thus reduced or eliminated.

[0027] The appropriate phase offsets can be established once or periodically, at power-up for example. An overall system approach can identify victim links by monitoring receiver bit-error rates. In one embodiment, one or more victim links are identified by determining which links have relatively high bit error rates. Links physically located near the victim link are identified and referred to as “likely aggressor links.” Likely aggressors can then be phase adjusted in the manner described above to minimize the bit-error rates of the victim receivers. Such an approach might focus on reducing the bit-error rate of the most noise-sensitive channels, or might attempt to minimize the bit-error rate for the entire system. Alternatively, collections of neighboring or related communication channels can be optimized in groups, as where the speed performance of a system depends heavily on a particular one or a subset of the communication channels. In another embodiment, a multi-variable optimization routine may be used to improve overall system performance. In one such embodiment, one or more victim links are identified by determining which links have relatively high bit error rates. The overall bit error rate of the system may also be determined. A number of likely aggressor links are identified, for example by physical proximity, and the timing of the data transmitted on these links is adjusted. The bit

error rates of the individual victim channel, the overall system, or both are then recalculated.

These steps are repeated until an optimal or acceptable per-channel or system-wide bit error rate is obtained.

[0028] Figure 3A depicts a plesiochronous system 300 in accordance with another embodiment. System 300 is similar to system 200 of Figure 2A, like-numbered elements being the same or similar. In a plesiochronous system, the communicating components do not share the same system clock. Each component may contain some clock-synthesis circuitry, which may include a phase-lock loop, to generate local clocks. In this example, clock synthesizers 247 and 248 develop respective local receive clocks LRC1 and LRC2 from respective local reference clocks CRef1 and CRef2. In Figure 3A, as in Figure 2A, and solely for illustrative purposes, channel 212 is depicted as the aggressor and channels 215 and 216 are depicted as the victims.

[0029] The techniques described above in connection with the mesochronous system 200 of Figure 2A can be applied to plesiochronous systems. The clocks used by aggressor transmitters and victim receivers to time the transmission and reception of signals in plesiochronous systems are not fixed in phase relative to each other because of the frequency differences of their respective local clocks. Because fixed clock alignment is unavailable in such cases, the phase-adjustment techniques discussed above for mesochronous systems do not apply to NEXT in plesiochronous systems. Transmitters on the same device in a plesiochronous system do share a common clock, however, so the relative phases of transmitted signals can be adjusted as discussed above in plesiochronous systems to reduce the impact of FEXT.

[0030] The systems of Figures 2A and 3A provide fixed, optimized phase relationships between transmitted data streams to reduce the impact of FEXT and NEXT in mesochronous systems and to reduce the impact of FEXT in plesiochronous systems. Another embodiment,

introduced below in connection with Figure 3B, reduces the impact of FEXT and NEXT in both mesochronous and plesiochronous systems.

[0031] Figure 3B is a waveform diagram 350 depicting a transmit data symbol 355 for the transmit data TXD1 associated with aggressor channel 212 of Figure 3A. Moving the timing of aggressor symbol 355 with respect to victim data eyes 360 of victim data on channel 216 reduces the likelihood that a given crosstalk artifact will be introduced coincident with the sampling instant on victim channel 216. Transmission errors that result from crosstalk may still occur on occasion, but such errors will tend to be spread out in time, as opposed to occurring in large numbers when system 300 encounters a particular phase relationship between local clock signals LRC1 and LRC2. This “phase walking” technique does not provide a fixed, optimized timing relationship, but instead reduces the probability of worst-case timing alignment, especially in a multi-aggressor environment by reducing the probability that multiple aggressor signals align in time to produce an additive deleterious effect on one or more victim channels.

[0032] Figure 4 depicts a transceiver 400 in accordance with another embodiment. For simplicity, transceiver 400 includes only two communication channels, one outgoing channel 402 and one incoming channel 403, but typical systems may include more. Transceiver 400 includes a transmit section 405, a receive section 407, and a phase-lock loop (PLL) 409 shared by both transmit and receive sections 405 and 407.

[0033] Receive section 407 is of a well-known type, and is thus not described in detail. In brief, receive section 407 includes a phase detector 425 and a sampler 411, each of which samples received data from channel 403. Phase detector 425 provides an output signal to a receiver phase controller 413, which controls the sample timing of the received signal via a phase mixer 415 that derives edge and data clocks EdClk and DaClk by combining selected ones of a plurality of differently phased reference clocks from PLL 409. Sampler 411, thus properly timed,

samples the incoming data and provides the resulting sampled data to a deserializer 422 for conversion to parallel input data InData.

[0034] Transmit section 405 is largely conventional, but is modified in accordance with one embodiment to allow for one-time, periodic, or continuous variation in the timing of the transmit clock TxClk. Transmit section 405 conventionally includes a resynchronizer 420 that re-times parallel transmit data TxData timed to a local clock LClk to transmit clock TxClk. The resulting re-timed parallel data TxDr is then fed to a serializer 423. Serial transmit data TxDs from serializer 423 is then conveyed to a transmitter 426 for transmission over channel 402. In one embodiment, resynchronizer 420 is of a type described in U.S. Patent Application Serial No. 10/282,531 entitled “Method and Apparatus for Fail-Safe Resynchronization with Minimum Latency,” which is incorporated herein by reference.

[0035] In addition to the foregoing conventional components, transmit section 405 includes a transmit phase mixer 430 controlled by transmit phase-control circuitry 435. Phase-control circuitry 435 may be a simple volatile or non-volatile register, in one embodiment, that can be loaded with different counts to adjust the phase of transmit clock TxClk. As discussed in connection with Figures 2A-2C, this count can be selected to minimize the impact of NEXT, FEXT, or both. In similar transmitters of other embodiments, phase controller 435 continuously or periodically alters the setting of phase mixer 430 to dynamically alter the timing of the transmitted signal or signals in the manner described in connection with Figure 3B. In one embodiment, for example, phase controller 435 includes a counter that continuously counts up and down between two extremes of phase position to continuously sweep the phase of data eyes transmitted on channel 402 at a rate below that of the receive data CDR. Phase controller 435 and phase mixer 430 are analog devices in other embodiments, and thus allow for a full spectrum of dynamic or fixed phase adjustments.

[0036] Of interest, some conventional transceivers similar to the one of Figure 4 include a transmit phase mixer between the PLL and transmit-clock line TxClk. One such system is shown, for example, in Figure 14 of an article entitled “Equalization and Clock Recovery for a 2.5-10-Gb/s 2-PAM/4-PAM Backplane Transceiver Cell,” by Jared L. Zerbe, et al. (IEEE JSSC, December 2003). The transmit phase mixer of that article is not adjustable, however, but is used only to match the delay of the transmit-clock path with the delay through the PLL feedback loop. Transmitters in accordance with the embodiments described herein add transmit phase-control circuitry to facilitate transmit phase adjustment.

[0037] Figure 5 (prior art) depicts a phase mixer 500 used in some embodiments of transceiver 400 as transmit phase mixer 430. Mixer 500 includes a first multiplexer 505, a second multiplexer 510, and an integrator 515. As is conventional, multiplexers 505 and 510 receive respective odd and even clock phases of a plurality of clocks derived from reference clock RefClk by PLL 409. Integrator 515 combines the selected odd and even phases to produce transmit clock TxClk. Similar mixers may be used for receive phase mixer 415.

[0038] Figure 6 depicts a communication system 600 in accordance with an embodiment in which a system phase controller 605 issues control signals Ctrl to a transmitter 610 based upon feedback signals received from one or more near-end receivers 615. Phase controller 605 can adjust the phase of data signals transmitted on one or more aggressor channels to minimize the impact of such data signals on victim channels. In the depicted example, system controller 605 controls the phase of data transmitted from transmitter 610 to a far-end receiver 620 to minimize the effects of NEXT on an adjacent victim data channel Rx DATA to receiver 615. Receiver 615 issues an error signal Err to controller 605, thus providing feedback upon which to base phase adjustments in transmitter 610. Error signal Err may carry a quality metric for the received data, such as a bit error rate, or the voltage margin, timing margin, or both to a particular bit error rate.

[0039] Figure 7 depicts a communication system 700 in accordance with an embodiment in which a system phase controller 705 issues control signals Ctrl to one or more potential aggressor transmitters 710 in response to feedback signals received from one or more far-end receivers 715. Phase controller 705 adjusts the phase of data signals transmitted on aggressor channels to minimize the impact of such data signals on victim channels. In the depicted example, system controller 705 controls the phase of data Data2 to minimize the effects of FEXT on data Data1 to receiver 715. Receiver 715 issues error signals Err to controller 705, thus providing feedback upon which to base phase adjustments.

[0040] Figure 8 depicts a multi-channel transmitter 800 that includes two (or more) collections of N transmitters 805 and 810. A first phase-adjust circuit 815 controls transmitters 805 and a second phase-adjust circuit 820 controls transmitters 810. The transmit channels from the separate collections are depicted as grouped together, but the physical channels may be overlapping, interleaved, etc. Transmitters 805 and 810 employ separate reference clocks RefClk1 and RefClk2, but may share a common clock. Further, transmitters 805 and 810 may be portions of the same or different integrated circuits and may be on the same or separate printed-circuit boards.

[0041] As noted above in connection with Figure 1, modern high-speed communication systems often include a complex matrix of densely populated communication channels. Some or all of the aggressor and victim transmitters may be provided with phase-adjustment circuits that can be optimized for a given noise environment. It may be sufficient, for example, to include phase adjustment for only of subset of potential aggressors and victims.

[0042] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the various depicted embodiments. In some instances, the terminology and symbols may imply specific details that

are not required to practice the invention. For example, the interconnection between circuit elements or circuit blocks may be shown or described as multi-conductor or single conductor signal lines. Each of the multi-conductor signal lines may alternatively be single-conductor signal lines, and each of the single-conductor signal lines may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described as being single-ended may also be differential, and vice-versa. Similarly, signals described or depicted as having active-high or active-low logic levels may have opposite logic levels in alternative embodiments.

[0043] While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. For example, while the foregoing embodiments reduce crosstalk in channels that extend between integrated circuits (ICs), the methods and circuits described herein can be adapted to reduce intra-IC crosstalk. Further, the timing of both the leading and trailing edges of transmitted data may be independently adjusted in some embodiments to reduce crosstalk effects. And, in still other embodiments, the crosstalk minimization schemes described herein are applied to asynchronous systems. Moreover, some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance the method of interconnection, or “coupling,” establishes some desired electrical communication between two or more circuit nodes, or terminals. Such coupling may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description. Only those claims specifically reciting “means for” or “step for” should be construed in the manner required under the sixth paragraph of 35 U.S.C. Section 112.